Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Previously Presented) A method in a data processing system for monitoring execution of instructions, the method comprising:

receiving a bundle at an instruction cache, the bundle containing an instruction;

responsive to receiving the bundle, determining whether the bundle contains an indicator, wherein the indicator identifies the instruction as one that is to be monitored by a performance monitor unit;

responsive to a determination that the bundle contains the indicator, incrementing a counter associated with the instruction wherein the incrementing provides a count of a number of times the instruction is executed; and

sending the bundle from the instruction cache to a functional unit for execution of the instruction.

2. (Previously Presented) The method of claim 1 further comprising:

resetting the counter if the counter exceeds a threshold value; and reading a value of the counter prior to the counter exceeding the threshold value.

3-5. Canceled.

6. (Original) The method of claim 1, wherein the counter is located in a shadow memory.

7 – 25. Canceled.

26. (Previously Presented) The method of claim 1 further comprising using a spare field in the bundle to contain the indicator.

27. (Previously Presented) The method of claim 1, further comprising:

responsive to a determination that the bundle contains the indicator, sending a signal to the performance monitor unit.

28. (Previously Presented) The method of claim 27, wherein the step of incrementing the counter associated with the instruction is performed by the performance monitor unit.

29. (Previously Presented) The method of claim 1, further comprising:

responsive to a determination that the bundle contains the indicator, beginning incrementing the counter, wherein the counter tracks any subsequent instruction executed by an associated processor.

30. (Previously Presented) The method of claim 29 wherein the bundle is a first bundle, the method further comprising:

receiving a second bundle at the instruction cache;

responsive to receiving the second bundle, determining whether the second bundle contains a second indicator; and

responsive to a determination that the second bundle contains the second indicator, ending incrementing the counter.

31. (Previously Presented) The method of claim 30, wherein the counter and the second counter are identical.

32. (Currently Amended) A computer program product comprising:

a computer readable, recordable-type medium having computer useable program code for monitoring execution of instructions, the computer program product comprising:

computer usable program code for receiving a bundle at an instruction cache, the bundle containing an instruction;

computer usable program code for, responsive to receiving the bundle, determining whether the bundle contains an indicator, wherein the indicator identifies the instruction as one that is to be monitored by a performance monitor unit;

computer usable program code for, responsive to a determination that the bundle contains the indicator, incrementing a counter associated with the instruction wherein the incrementing provides a count of a number of times the instruction is executed; and

computer usable program code for, sending the bundle from the instruction cache to a functional unit for execution of the instruction.

33. (Previously Presented) The computer program product of claim 32 further comprising:

computer usable program code for resetting the counter if the counter exceeds a threshold value; and

computer usable program code for reading a value of the counter prior to the counter exceeding the threshold value.

34. (Previously Presented) The computer program product of claim 32, wherein the computer usable program code for incrementing the counter further comprises computer usable program code for incrementing the counter, wherein the counter is located in a shadow memory.

35. (Previously Presented) The method of claim 32 further comprising using a spare field in the bundle to contain the indicator.

36. (Previously Presented) The computer program product of claim 32, further comprising:

computer usable program code, responsive to a determination that the bundle contains the indicator, for sending a signal to the performance monitor unit.

37. (Previously Presented) The computer program product of claim 36, wherein the computer usable program code for incrementing the counter associated with the instruction computer usable program code to be executed on the performed by the performance monitor unit.

38. (Previously Presented) The computer program product of claim 32, further comprising:

computer usable program code, responsive to a determination that the bundle contains the indicator, for beginning incrementing the counter, wherein the counter tracks any subsequent instruction executed by an associated processor.

39. (Previously Presented) The computer program product of claim 38 wherein the bundle is a first bundle, the computer program product further comprising:

computer usable program code for receiving a second bundle at the instruction cache;

computer usable program code, responsive to receiving the second bundle, for determining whether the second bundle contains a second indicator; and

computer usable program code, responsive to a determination that the second bundle contains the second indicator, for ending incrementing the counter.

40. (Previously Presented) The computer program product of claim 39, wherein the counter and the second counter are identical.

41. (Previously Presented) A data processing system comprising:

a bus;

a communications unit connected to the bus;

a storage device connected to the bus, wherein the storage device includes computer usable program code; and

a processor unit connected to the bus, wherein the processor unit executes the computer usable program code to receive a bundle at an instruction cache, the bundle containing an instruction, responsive to receiving the bundle, to determine whether the bundle contains an indicator, wherein the indicator identifies the instruction as one that is to be monitored by a performance monitor unit, responsive to a determination that the bundle contains the indicator, to increment a counter associated with the instruction wherein the incrementing provides a count of a number of times the instruction is executed, and to send the bundle from the instruction cache to a functional unit for execution of the instruction.

42. (Previously Presented) The data processing system of claim 41, wherein the processor unit further executes computer usable program code to reset the counter if the counter exceeds a threshold value, and to read a value of the counter prior to the counter exceeding the threshold value.

43. (Previously Presented) The data processing system of claim 41, wherein the processor unit executing computer usable program code to increment the counter further comprises executing computer usable program code to increment the counter, wherein the counter is located in a shadow memory.

44. (Previously Presented) The data processing system of claim 41 wherein the processor unit further executes computer usable program code to use a spare field in the bundle to contain the indicator.

45. (Previously Presented) The data processing system of claim 41, wherein the processor unit further executes computer usable program code, responsive to a determination that the bundle contains the indicator, to send a signal to the performance monitor unit.

46. (Previously Presented) The data processing system of claim 45, the computer usable program code for incrementing the counter associated with the instruction computer usable program code to be executed on the performed by the performance monitor unit.

47. (Previously Presented) The data processing system of claim 41, wherein the processor unit further executes computer usable program code, responsive to a determination that the bundle contains

the indicator, to begin incrementing the counter, wherein the counter tracks any subsequent instruction executed by an associated processor.

48. (Previously Presented) The data processing system of claim 47 wherein the bundle is a first bundle, wherein the processor unit further executes computer usable program code to receive a second bundle at the instruction cache, responsive to receiving the second bundle, to determine whether the second bundle contains a second indicator, and responsive to a determination that the second bundle contains the second indicator, to end incrementing the counter.